

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,177,196 B2  
APPLICATION NO. : 10/073999  
DATED : February 13, 2007  
INVENTOR(S) : Ken Takeuchi et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, References Cited section (56), Foreign Patent Documents:

Please insert the following references:

--JP	11-17619	07/1999
JP	11-167800	06/1999
CN	1211040A	03/1999--

In Column 101, Claim 5, Line 1:

Please replace "bit connected" with --bit line connected--

In Column 101, Claim 5, Line 21:

Please replace "second memory cell" with --second bit line is latched in said common latch circuit and a verify read operation to verify whether said second memory cell--

In Column 101, Claim 10, Line 59:

Please insert --a second bit line;--

In Claim 11, Column 102, Line 31-Column 103, Line 4:

Please replace Claim 11 with the following:

--The nonvolatile semiconductor memory according to claim 10, wherein said first and second memory cells are connected to a same word line.--

In Claim 12, Column 102, Lines 5-8:

Please replace Claim 12 with the following:

--The nonvolatile semiconductor memory according to claim 11, wherein while said program/read data is held by said first, second, third, or fourth bit line, a potential of a bit line adjacent to said first, second, third, or fourth bit line is set at a fixed potential.--

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In Claim 13, Column 104, Lines 1-6:

Should read as follows:

--The nonvolatile semiconductor memory according to claim 12, wherein said fixed potential is a ground potential or a power supply potential.--

Signed and Sealed this

Twenty-ninth Day of July, 2008

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS  
*Director of the United States Patent and Trademark Office*